Amendments to the Drawings

Please replace sheet 3 of 4 containing Figs. 5 and 6 with the Replacement Sheet 3 of 4 enclosed herein.

Remarks

Claims 2, 8, and 23 have been amended. Support for these amendments is found in the specification and drawings. Thus, no new matter has been added. Claims 2, 8, 16, and 23 are pending in the present application.

Amendment to the Drawings

Applicants have amended the drawings to reflect what is described on page 14, lines 11-16 of the specification, and described in the original claims, for example original claims 2 and 16. Thus, no new matter has been added. Accordingly, an amended paragraph has been enclosed herein.

Amendment to the Specification

Applicants have amended the Cross Reference To Related Applications section on page 1 to list the related applications and update the applications status. Also, Applicants have amended page 14, lines 11-16 of the specification to describe what was shown in Fig. 6 and describe in the original claims, for example original claims 2 and 16. Thus, no new matter has been added. Accordingly, an amended paragraph has been enclosed herein.

Rejection under § 112

Claims 2, 8, 16, and 23 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. The Examiner asserted that it is unclear as to the metes and bounds of the limitation "capacitor accommodated in a space defined by a thickness dimension of a topographic contact". Accordingly, Applicants have amended claims 2 and 8 to delete the limitation "capacitor accommodated in a space defined by a thickness dimension of a topographic contact" and replace it with the limitation wherein "a thickness dimension (a) of the decoupling capacitor is less than or equal to a thickness dimension (b) of a topographic contact" (claims 2 and 8) or "a thickness dimension (a) of the decoupling capacitor is less than or equal to either a thickness dimension (b) of a topographic contact or a thickness dimension (c) of the first semiconductor die". Thus, Applicants respectfully request the withdrawal of the rejection of these claims under 35 U.S.C. 112. As claim 16 depends from claim 2, Applicants request the withdrawal of the rejection under 35 U.S.C. 112 of this claim as well.

Applicants submit that contrary to the Examiner's assertion, claim 23 does not include the limitation "capacitor accommodated in a space defined by a thickness dimension of a topographic contact". Thus, Applicants respectfully request the rejection under 35 U.S.C. 112 of claim 23 be withdrawn.

Rejection under § 103

Claims 2 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al (US 6,507,098) in combination with Distefano (US 6,075,289) and Suzuki et al (US 5,532,910). Claim 16 remains rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al, Distefano and Suzuki et al as applied to claim 2 and further in combination with Corisis et al (US 2002/0135066). Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al in combination with Distefano, Suzuki et al and Searls (US 2004/0155335; newly cited reference). Applicants respectfully traverse the rejections of the claims and submit that the burden of establishing a prima facie case of obviousness under §103 has not been met. *MPEP §2145.*

In order to establish a prima facie case of obviousness under §103, the Examiner has the burden of showing, by reasoning or evidence, that: 1) there is some suggestion or motivation, either in the references themselves or in the knowledge available in the art, to modify that reference's teachings; 2) there is a reasonable expectation on the part of one of ordinary skill in the art that the modification or combination has a reasonable expectation of success; and 3) the prior art references (or references when combined) teach or suggest all the claim limitations. *MPEP §2145.* The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Independent claims 2, 8, and 23 recite a printed circuit board assembly comprising, *inter alia*, a first semiconductor die, a second semiconductor die, an intermediate substrate positioned between the first semiconductor die and the second semiconductor die, a heat sink mounted to the substrate, and a decoupling capacitor mounted to the substrate, wherein a thickness dimension (a) of said decoupling capacitor is less than of either a thickness dimension (b) of a topographic contact (claims 2, 8, and 23) or a thickness dimension (c) of the first semiconductor die (claim 23).

Applicants respectfully submit that Lo et al., Distefano, Suzuki et al., Corisis et al., or Searls teach, suggest, or motivate, singularly or in combination, a decoupling capacitor mounted to an intermediate substrate within a stacked chip arrangement, wherein a thickness dimension (a) of the capacitor is less than either a thickness dimension (b) of a topographic contact or a thickness (c) of a first semiconductor die as recited in Applicants' claims. The Examiner acknowledges that Lo does not disclose a heat sink coupled to a intermediate substrate, or at least one decoupling capacitor mounted to an intermediate substrate, or wherein a thickness dimension (a) of the decoupling capacitor is less than either a thickness dimension (b) of the respective topographic contact or a thickness dimension (c) of the first semiconductor die (i.e., "wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of a topographic contact or first semiconductor die").

In order to alleviate this deficiency in Lo's teachings, the Examiner asserts that Suzuki teaches a decoupling capacitor accommodated in a space, mounted on an intermediate substrate and coupled to a die. However, Suzuki et al. teach the capacitor is mounted to a lead frame, not an intermediate substrate, so as to be connected in series with the output terminals of a IC chip and sealed in mold resin (22). (Col. 1, lines 48-50). In fact, nowhere does Suzuki et al. teach or suggest, singularly or in combination with Lo et al. or any other reference, a capacitor mounted to an intermediate substrate, let alone, wherein its thickness dimension (a) is less than the thickness dimension (b) of the topographic contact or the thickness dimension (c) of the first semiconductor die.

Thus, lacking such a teaching or suggestion, the Examiner asserts "With respect to the placement of the capacitor, such that it is mounted on the intermediate substrate, or that a thickness dimension of one of said first semiconductor1, it would have been obvious, since the rearrangement[s] of parts have been held unpatentable **absent** a **showing** of **criticality** or unexpected results. See e.g. *In re Japiske*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950) (claims held unpatentable because shifting the position of the starting switch would not have modified the operation of the device); see also *In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice)." The Examiner then asserts that no showing of motivation to rearrange is necessary because legal precedent can provide the rational supporting obviousness of the

modification because in the present application, it has been held that mere rearrangement of parts is prima facie case obviousness absent a showing of criticality. (MPEP 2144 [R-5]).

Applicants respectfully submit that there has been a showing of criticality within Applicants' specification regarding the placement of components, such as the capacitor, within a stacked chip arrangement. For example, the Applicants' state that increased miniaturization of components and greater packaging density of integrated circuits are ongoing goals of the computer industry. (Application, p. 2, lines 25-26). Moreover, Applicants state "However, greater integrated circuit density is primarily limited by the space or 'real estate' available for mounting dies on a substrate, such as a printed circuit board." (Application, p. 3, lines 7-9). Applicants further state "Despite the advantages of the most recent developments in semiconductor fabrication there is a continuing need for improved schemes for increasing semiconductor die density in printed circuit board assemblies." (Id. at lines 12-15). Thus, Applicants submit that since the 'real estate' or space available for mounting dies on a substrate is limited and impacts the integrated circuit's density, then clearly the position of the capacitor on the substrate, which also will take up available 'real estate' or space on the substrate, is critical to the present invention.

Also, complicating the design and arrangement of the stacked chip arrangement of the present invention, Applicants state that it is preferred that the capacitor be positioned as close as possible to at least one of the semiconductor dies. (Id. p. 13, lines 1-3). Thus, the mounting of the capacitor on the substrate provides a balance between the limited 'real estate' available for mounting the semiconductor dies and the capacitor with the desire to mount the capacitor as close to the dies as possible. Therefore, Applicants respectfully submit that contrary to the Examiner's assertions, the criticality of the limitations "the capacitor is mounted to the intermediate substrate" and "the capacitor has a thickness dimension (a) that is less than a thickness dimension of either a topographic contact or semiconductor die" has been shown because the capacitor's placement and size impacts the density of a stacked chip arrangement. Therefore, such limitations are **more than a mere obvious rearrangement of parts**.

Furthermore, in order to rely on legal precedent, MPEP 2144 requires "If the facts in a prior legal decision are sufficiently similar to those in an application under examination, the examiner may use the rationale used by the court." MPEP 2144. In the instant case, the Examiner has proffered no evidence that the facts of the relied upon prior legal decisions are

sufficiently similar to the present case. Applicants submit that in the instant case, depending upon where the capacitor is placed within the stacked chip arrangement, the stack height, density, and space availability will be affected. This is sufficiently different than the placement of a starting switch on a hydraulic press or a contact in a conductivity measuring device wherein no concern of density, size, or space has been expressed.

"The mere fact that a worker in the art could rearrange the parts of the reference device to meet the terms of the claims on appeal is not by itself sufficient to support a finding of obviousness. The **prior art must provide** a **motivation or reason** for the worker in the art, without the benefit of appellant's specification, **to make the necessary changes** in the reference device." (emphasis added) *Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984); see also MPEP §2144.04 (VI)(C). Additionally, the Federal Circuit has stated, "The mere fact that prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. It is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious." *In re Fritsch*, 23 USPQ2d 1780, 1783-4 (Fed. Cir. 1991).

Having made a showing of criticality of the placement of the capacitor, Applicants respectfully submit that the references provide no such required motivation or reason to mount the capacitor of Suzuki et al. on the substrate of Lo et al., let alone that the thickness dimension of the capacitor is less than the thickness dimension of either the topographic contact or semiconductor die as recited by Applicants claims. All the references, i.e., Lo et al., Suzuki et al., Distefano, Corisis, and Searls are silent, singularly or in combination, as to mounting capacitors in such a stacked chip arrangement, particularly wherein its thickness is less than the thickness of either the topographic contact or semiconductor die. Moreover, none of the references, singularly or in combination, teach or suggest the capacitor conductively coupled to either the first or second semiconductor dies. These are explicitly claimed limitations that the Examiner has not shown as taught explicitly or implicitly in the art. Lacking the necessary teaching, motivation, or suggestion, Applicants respectfully submit that the Examiner has arbitrarily made the necessary changes in the reference devices to come up with Applicants' claimed invention. Thus, Applicants believe the Examiner has mistakenly used Applicants'

specification as a "template" to piecemeal the teachings of the prior art to reject Applicants' independent claims.

Therefore, Applicants respectfully submit that the none of the references, singularly or in combination, teach or suggest all of the limitations of Applicants' claims 2, 8, and 23. Accordingly, the required burden of a prima facie case of obviousness has not been met, and the Applicants respectfully request that the rejections under 35 U.S.C. §103 of independent claims 2, 8, and 23 be withdrawn. As claim 16 depends from independent claim 2, the rejection of this claim under 35 U.S.C. §103 should be withdrawn as well. Thus, the Applicants respectfully submit that, in view of the above amendments and remarks, the application is now in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully requested.

Respectfully submitted,
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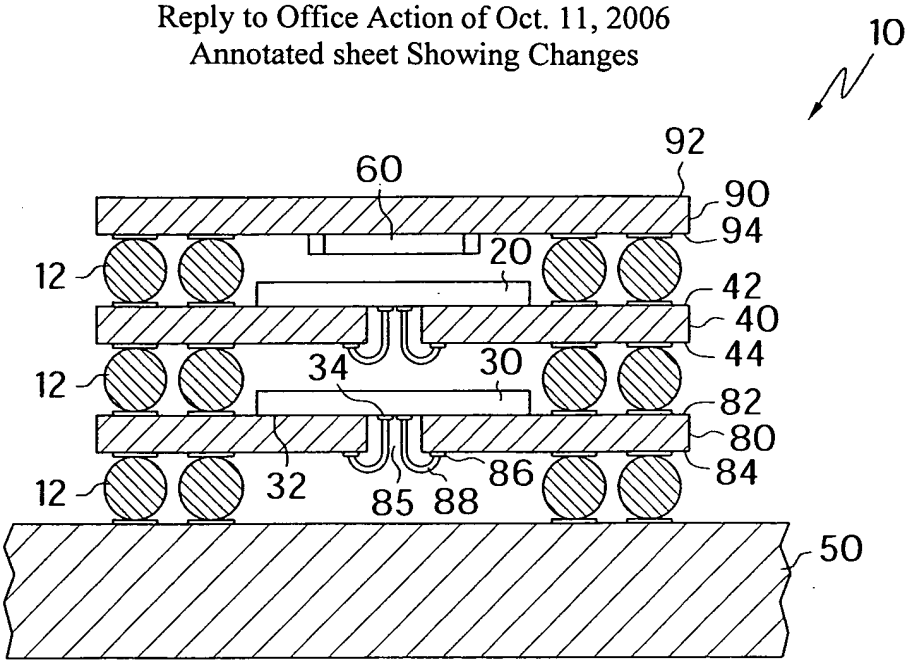

FIG. 5

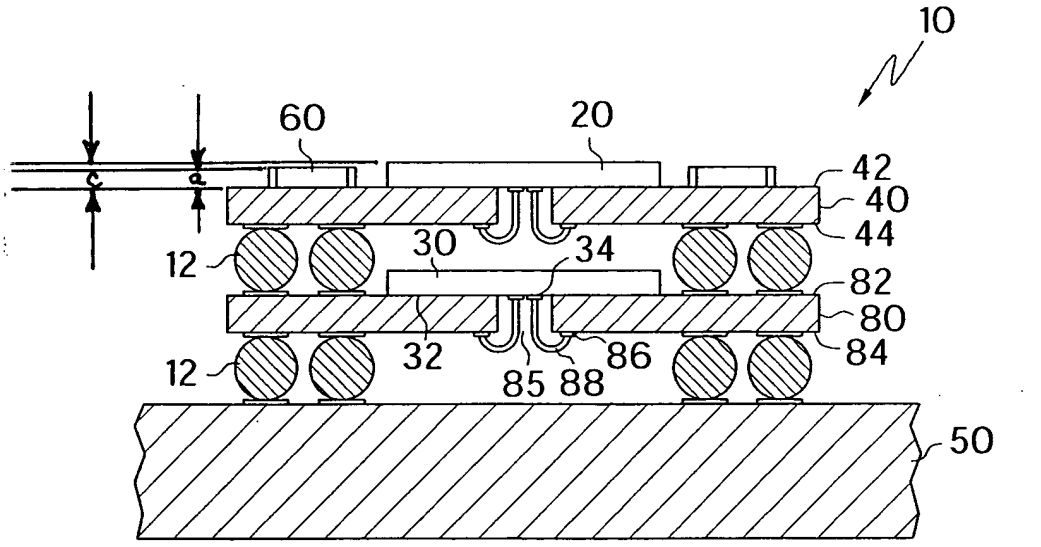

FIG. 6